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UNITED STATES PATENT APPLICATION FOR:

METHOD OF AND APPARATUS FOR MEASURING THE CORRECTNESS OF AND CORRECTING AN AUTOMATIC TEST ARRANGEMENT

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METHOD OF AND APPARATUS FOR MEASURING THE CORRECTNESS OF AND CORRECTING AN AUTOMATIC TEST ARRANGEMENT

FIELD

[0001] The present invention pertains to automatic test arrangements for automatic testing of devices. More particularly, the present invention pertains to a method of and an apparatus for determining the correctness of the calibration of an automatic test arrangement and a method of and apparatus for correcting the fundamental calibration errors inherent in automatic test equipment, arrangements, and/or environments.

BACKGROUND

[0002] Newly manufactured products are generally tested prior to being delivered to customers in order to assure that the products perform as desired. In high volume manufacturing of products, such as electronic components, such acceptance testing is often performed by automatic test equipment. The test results, however, are only as good as the calibration of the automatic test equipment. This is a problem in general in acceptance testing, and it is a particular and fundamental problem in the acceptance testing of electronic components since the available operating speeds of such components are increasing, and the component operating speed is often faster than the operating speed of the automatic test equipment. Methods of calibration presently used, known, and/or available are limited in accuracy and have associated inherent errors. Consequently, in order to accurately evaluate and correct the results of testing by automatic test equipment, it is necessary to determine the correctness of the calibration of the automatic test

equipment and to make and/or embed any modification and/or corrections to the base tester calibration and/or the test results that are necessary to obtain meaningful results.

[0003] The present invention is applicable to automatic test equipment, automatic test arrangements, and automatic test environments. In the following, these will all be referred to as automatic test arrangements, but it is to be understood that equipment, arrangements, and environments are included, as well as other appropriate meanings.

[0004] Figure 1 is a block diagram commonly considered to depict an automatic test arrangement testing a device. Tester driver 10 applies a test signal to pin electronics card 12, the output of which is connected to the input of tester interface unit 16. The output of tester interface unit 16 is connected to the device under test 20. Tester driver 10, and pin electronics card 12, might be a piece of general purpose automatic test equipment, while tester interface unit 16 is specifically adapted for testing of the particular device under test 20 on such a general purpose automatic test equipment.

[0005] The automatic test arrangement of Figure 1 can test device under test 20 by determining the electrical length of the signal path from tester driver 10 to device under test 20, using time domain reflectometry. A signal is applied from tester driver 10, through pin electronics card 12 and tester interface unit 16 to device under test 20, and a resulting reflected signal is returned to tester driver 10. The time between initiation of the signal by tester driver 10 and receipt of the reflected signal at tester driver 10 is used to determine whether device under test 20 is acceptable, as is well known in the art. That time is referred to as the electrical length of the signal path.

[0006] In practice the automatic test arrangement is calibrated with no device connected to the output of tester interface unit 16. This calibration electrical length is:

$$EL = PEC + TIU$$

where EL is electrical length, PEC is the electrical length of pin electronics card 12, and TIU is the electrical length of tester interface unit 16. This electrical length might be determined under various conditions. One condition is with no ground connections. A second is with the output of tester interface unit 16 connected to ground by a grounding block. A third condition is with the output of pin electronics card 12 connected to ground by a first grounding block and the output of tester interface unit 16 connected to ground by a second grounding block. While each of these methods produces a calibration value for the automatic test arrangement, the calibration values differ, and, in fact, none of them is wholly accurate because none of them considers all of the electrical lengths involved in the test arrangement. Nevertheless, these three conditions are frequently used variously to calibrate automatic test equipment.

[0007] The electrical length of the automatic test equipment made up of tester driver 10 and pin electronics card 12 is generally tested to obtain a first calibration value which might be stored in a memory device of the pin electronics card. Because not all electrical lengths are considered, the measured value is the actual electrical length of the pin electronics card plus a calibration adjustment. One such value might be obtained and stored with the output of the pin electronics card open and another value obtained and stored with that output shorted to ground.

[0008] A second set of calibrations is generally performed to determine the electrical length of the pin electronics card and the tester interface unit, both with the tester interface unit output open, and with that output shorted to ground, and the resulting values might be stored in a memory device of the tester interface unit. Again, however,

the measured values are the electrical length of the pin electronics card and the tester interface unit plus a calibration adjustment. Even so, these stored values do not properly reflect the calibration of the automatic test arrangement because they do not take into consideration all the electrical lengths involved. Consequently, it is difficult to correctly calibrate an automatic test arrangement.

SUMMARY

[0009] The present invention pertains to automatic test arrangements for automatic testing of devices. More particularly, the present invention pertains to a method of and an apparatus for determining the correctness of the calibration of an automatic test arrangement and a method of and an apparatus for correcting fundamental calibration errors inherent in an automatic test arrangement. Such an automatic test arrangement generally includes a tester driver, a pin electronics card having an input connected to the tester driver and an output connected to an output pin such as pogo pin, and a tester interface unit having an input connected to the pin electronics card output pin and an output connected to an output pin such as a socket pin. In accordance with the present invention, the electrical length from the tester driver to the socket pin is determined taking into consideration the pin electronics card output pin and the tester interface unit output pin. The actual electrical length from the tester driver, through the pin electronics card, the pin electronics card output pin, the tester interface unit, and the tester interface unit output pin to a grounding point of the device under test is determined. In a first embodiment of the invention, a second electrical length is determined from the tester driver, through the pin electronics card and the pin electronics card output pin to the

tester interface unit, with neither the pin electronics card output pin nor the tester interface unit output pin grounded. With the tester interface unit output pin connected to ground by a shorting block, a third electrical length is determined from the tester driver, through the pin electronics card, the pin electronics card output pin, the tester interface unit, the tester interface unit output pin, and the shorting block to ground. A first difference value is determined as the difference between the first electrical length and the second electrical length. A second difference value is determined as the difference between the first electrical length and the third electrical length. A third difference value is determined as the difference between the first difference value and the second difference value, and the third difference value is evaluated to determine the correctness of the calibration of the automatic test arrangement.

[0010] In another embodiment of the invention, a fourth electrical length is determined with the pin electronics card output pin connected to ground by a first shorting block and the tester interface unit output pin connected to ground by a second shorting block, the fourth electrical length being from the tester driver, through the pin electronics card, the pin electronics card output pin, the tester interface unit, the tester interface unit output pin, and the second shorting block to ground. A difference value is determined as the difference between the first electrical length and the fourth electrical length. This difference value is subtracted from the first difference value, and that result is evaluated to determine the correctness of the calibration of the automatic test arrangement.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] These and other aspects and advantage of the present invention are more apparent from the following detailed description and claims, particularly when considered in conjunction with the accompanying drawings. In the drawings:

[0012] Figure 1 is a block diagram commonly considered to depict an automatic test arrangement testing a device;

[0013] Figure 2 is a block diagram depicting an actual automatic test arrangement testing a device;

[0014] Figure 3 is a flowchart of a first embodiment of a method of determining the correctness of the calibration of an automatic test arrangement in accordance with the present invention;

[0015] Figure 4 is a flowchart of a second embodiment of a method of determining the correctness of the calibration of an automatic test arrangement in accordance with the present invention; and

[0016] Figure 5 is a block diagram of a preferred embodiment of apparatus for determining the correctness of an automatic test arrangement in accordance with the present invention.

DETAILED DESCRIPTION

[0017] Figure 2 is a block diagram of an automatic test arrangement in which a tester driver 10 applies a test signal to pin electronics card 12, the output of which is connected to output pin 14. The input of tester interface unit 16 is connected to pin electronics card output pin 14, while the output of tester interface unit 16 is connected to output pin 18

which is connected to the device under test 20. By way of examples, output pin 14 from pin electronics card 12 might be a pogo pin, while output pin 18 from tester interface unit 16 might be a socket pin. Tester driver 10, pin electronics card 12, and pogo pin 14 might be a piece of general purpose automatic test equipment, while tester interface unit 16 and its socket pin 18 are specifically adapted for testing of the particular device under test 20 on such a general purpose automatic test equipment. The actual electrical length from tester driver 10 to device under test 20 in Figure 2 is given by:

$$EL(1) = PEC + Pogo\_c + TIU + Socket\_pin + \text{Shortest return path to ground} \quad (1)$$

where Pogo-c is the electrical length of pogo pin 14 when it is compressed, and Socket_pin is the electrical length of socket pin 18.

[0018] When the test arrangement is calibrated, the device under test 20 is not connected, and instead the socket pin is left open. In that configuration, the electrical length from tester driver 10 to socket pin 18 is given by:

$$EL(2) = PEC + Cal\_adj\_o + \{PEC + Pogo\_c + TIU - (PEC + Cal\_adj\_o)\} \quad (2)$$

where Cal_adj_o is the previously determined calibration adjustment value. TIU – (PEC + Cal_adj_o) might be stored in a memory device in tester interface unit 16.

[0019] With a shorting block connecting socket pin 18 to ground, the electrical length from tester driver 10 to ground through the shorting block is given by:

$$EL(3) = PEC + Cal\_adj\_o + \{PEC + Pogo\_c + TIU + Socket\_pin + Shrt\_blk\_dut - PEC - Cal\_adj\_o\} \quad (3)$$

where Shrt_blk_dut is the electrical length of the shorting block connected to socket pin 18.

[0020] With a first shorting block connecting pogo pin 14 to ground and second shorting block connecting socket pin 18 to ground, the electrical length from tester driver 14 to ground through the socket pin shorting block is given by:

$$EL(4) = \{PEC + Pogo\_c + Shrt\_blk\_pogo + Cal\_adj\_s\} + \{PEC + Pogo\_c + TIU + Socket\_pin + Shrt\_blk\_dut - PEC - Pogo\_c - Shrt\_blk\_pogo - Cal\_adj\_s\} \tag{4}$$

where Shrt_blk_pogo is the electrical length of the shorting block at pogo pin 14 and Cal_adj_s is a previously determined calibration adjustment value for the automatic test arrangement with shorting blocks on both pogo pin 14 and socket pin 18.

[0021] The values EL(1) through EL(4) are determined for an automatic test arrangement and are used to determine the correctness of the calibration of the automatic test arrangement. Figure 2 is a flowchart of a first embodiment of a method of determining the correctness of the calibration of an automatic test arrangement in accordance with the present invention. In step S1, the method is started. In step S2, the first electrical length is measured, utilizing equation (1). Then in step S3 the second electrical length is measured utilizing equation (2), and in step S4 the third electrical length is measured, using equation (3). In step S5, the second electrical length is subtracted from the first electrical length, giving:

$$\Delta 1 = EL(1) - EL(2) = Socket\_pin + \text{Shortest return path to ground} \tag{5}$$

[0022] In step S6, the third electrical length is subtracted from the first electrical length, giving:

$$\Delta 2 = EL(1) - EL(3) = \text{Shortest return path to ground} - Shrt\_blk\_dut \tag{6}$$

[0023] In step S7, the result of equation (6) is subtracted from the result of equation (5), giving:

$$\Delta 3 = \Delta 1 - \Delta 2 = \text{Socket\_pin} + \text{Shrt\_blk\_dut} \tag{7}$$

[0024] In step S8 this difference value is evaluated to determine whether the automatic test environment is acceptable. The socket pin electrical length is known from the socket specifications, while the electrical length of the shorting block for the device under test can be determined by measurement of the size of the shorting block, with the electrical length being, for example, 6ps/mm x the socket length. By comparing this calculated electrical length with the result of equation (7), the correctness of the calibration of the automatic test environment can be determined. If the correctness is not satisfactory, then in step S9 adjustments, corrections, and/or improvements are made, and the process returns to step S2 to determine whether the result is acceptable. By way of example, tester driver 10, pin electronics card 12, and/or tester interface unit 16 might be adjusted or their design improved. If the correctness of the calibration, although not exact, is nevertheless within tolerances, corrections can be made to the results obtained during acceptance testing in order to obtain corrected results. Once an acceptable difference Δ3 is obtained in step S8, the method ends in step S10.

[0025] Figure 3 is a flowchart of a second embodiment of a method for determining the correctness of the calibration of an automatic test environment in accordance with the present invention. The method of Figure 3 differs from the method of Figure 2 in steps S6 and S7. In step S6 the fourth electrical length is subtracted from the first electrical length, giving:

$$\Delta 2' = EL(1) - EL(4) = \text{Shortest return path to ground} - \text{Shrt\_blk\_dut} \tag{8}$$

[0026] That result is then subtracted from the result of equation (5), giving:

$$\Delta 3' = \Delta 1 - \Delta 2' = \text{Socket\_pin} + \text{Shrt\_blk\_dut} \tag{9}$$

[0027] Equations 6 and 8 are identical, and so equations 7 and 9 are also identical. Thus, the method of Figure 2 gives the same result as the method of Figure 3. The method of Figure 3, however, requires an additional shorting block for the pogo pin. In practice, for any given automatic test environment the decision of whether to use the method of Figure 2 or the method of Figure 3 might be based on the method that gives the greatest repeatability.

[0028] The calibration of an automatic test arrangement can be determined by the present invention. An automatic test equipment or a tester interface unit can have the ability to determine $\Delta 3$ built in so that the calibration of the arrangement can be checked when desired. As depicted in Figure 5, the present invention can also be implemented by a properly programmed automatic processing system 22 connected to the automatic test environment 24.

[0029] Although the present invention has been described with reference to preferred embodiments, various alternations, rearrangements, and substitutions can be made, and still the result would be within the scope of the invention.

What is claimed is: